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PATENT ABSTRACTS OF JAPAN

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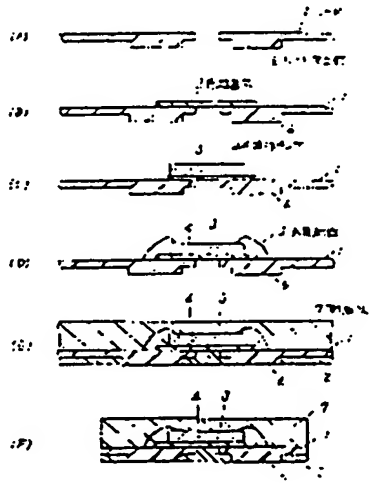
(71)Applicant : MATSUSHITA ELECTRIC IND CO LTD
(72)Inventor : KITAHIRO ISAMU
KONDO SHUJI
KIKUCHI TATSUO
TAKASE YOSHIHISA

(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:
PURPOSE: To obtain a highly accurate and highly reliable semiconductor device by placing a semiconductor chip through an insulating substrate on one group of highly accurate metal leads, connecting the leads to fine metal wirings, and transfer molding them.
CONSTITUTION: A thin resin plate 3 is attached to leads 1 having protrusions 6, and electrodes on a semiconductor chip 4 are connected to the leads 1 by fine metal wirings 5. Then, the leads except the protrusions 6 are sealed with resins 2, 7, shape and size are determined and cut. According to this structure, a small-sized and thin semiconductor device having high dimensional accuracy and reliability is obtained without complicated structure like a both-side substrate only by employing metal leads of special shape at part, and is freferably adapted for an IC.



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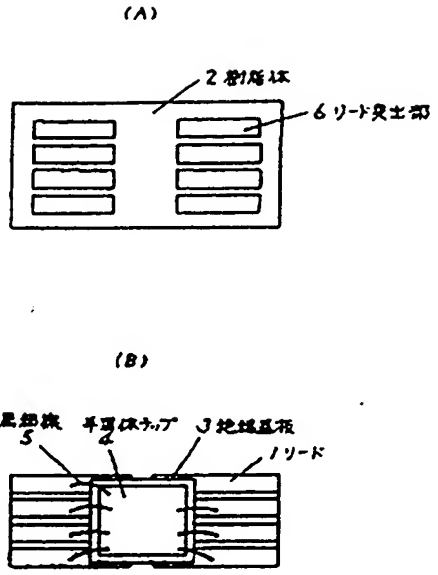

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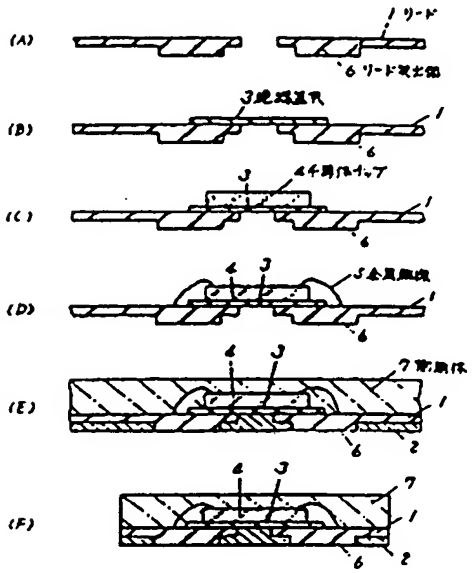

第 4 図